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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/987,884	11/16/2001	Yoshihiro Ikeda	XA-9582	7583

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER
SCHILLINGER, LAURA M

ART UNIT	PAPER NUMBER
2813	6

DATE MAILED: 11/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/987,884	IKEDA ET AL.	
	Examiner	Art Unit	
	Laura M Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/20/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the Election/Amdmt A in Paper No.5, dated 9/20/02.

Election/Restrictions

Claims 1-10 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto et al ('548).

In reference to claim 11, Hashimoto teaches a method for manufacturing a semiconductor IC including a MIS transistor structure comprising:

a) forming a first gate insulating film for forming the MIS transistor structure on a main surface of the semiconductor substrate (Fig.25b (31));

b) forming at least one pair of laminating structure bodies each including two layers of a first gate electrode (32 and 39) covering a part of the first gate insulating film (31) and a first

insulating film covering the first gate electrode (41), an etching prevention film being formed on a sidewall portion of the first insulating film(Col.10, lines: 25-27-see also Col.6, lines: 55-60);

c) introducing impurities into the semiconductor substrate through the first gate insulating film located in a region uncovered with the laminating structure bodies, and thereby forming a first impurity introduced region self-aligned with the laminating structure bodies on the main surface of the semiconductor substrate (Col.9, lines: 50-60 and Fig.22(a) and see also Fig.s 23 and 26 a) (38));

d) removing the first gate insulating film in the region uncovered with the laminating structure bodies after step (c) (Fig.26a- uncovered regions are not 31 (gate insulating layer but rather are FOX regions 30); and

e) forming a second insulating film covering upper portions and sidewall portions of the laminating structure bodies after step (d) (Fig.26 a and Col.10, lines: 25-27- 41 is an oxide-nitride-oxide film).

In reference to claim 12, Hashimoto teaches further comprising:
(d-2) oxidizing the main surface of the substrate in a region from which the first gate insulating film is removed, and thereby forming an insulating film on the main surface between steps (d) and (e) (Fig.22 a (30)).

In reference to claim 13, Hashimoto teaches further comprising the steps of :
f) forming a third insulating film over the second so as to cover the laminating structure bodies and embed each space between the laminating structure bodies (Fig.37 (a) (55));

g) forming a mask for a contact hole over the third film and selectively removing the third insulating film and the second insulating film in a laminating direction thereof by anisotropic etching using the mask and forming the contact hole which penetrates the third insulating film and the second insulating film which reaches a surface of a first impurity region (Col.12, lines: 50-55- see also Fig. 39a).

In reference to claim 14, Hashimoto teaches further comprising the step of :
h) forming a wiring conductive layer embedding the contact hole and electrically connected to the first impurity region (Fig.40-1a (58)).

In reference to claim 15, Hashimoto teaches wherein a second gate electrode and a second gate electrode laminated on an upper portion thereof are interposed between the first gate electrode and first gate insulating film constituting each of the laminating structure bodies (Fig. 38 a(50- floating gate and 55a is the control gate)).

In reference to claim 16, Hashimoto teaches wherein the first gate insulating film, and the third insulating film consist of silicon oxide (Col.11, line30- 31 is an oxide and Col.12, lines: 50-55 teaching 55' is an oxide) and the etching prevention film and the second insulating film each consist of silicon nitride (Col.6, lines: 54-56 teaching SiN is an etch stopper and Col.12, lines: 1-5- teaching the second insulating film is an O-N-O layer).

In reference to claim 17, Hashimoto teaches wherein the first and second gate electrodes consist of polycrystalline silicon (Col.11, lines: 50-65 teaching that floating gate 50 is polysilicon and Col.12, lines: 30-40- the control gate is polysilicon) and the second gate insulating film is an ONO layer (Col.12, lines; 1-5).

In reference to claim 18, Hashimoto teaches wherein the first insulating film consists of two films in which a silicon oxide and nitride film are laminated and the etching prevention film is formed to cover a sidewall portion of the two layer film (Col.6, lines: 50-60- teaching a (12) is a silicon oxide and (13) is a Silicon nitride).

In reference to claim 19, Hashimoto teaches a method comprising the steps of:

a) forming on a main surface of a semiconductor substrate, a first gate insulating film consisting of a SiO film (31), a second gate insulating film (51) and a second conductive film (55A) over the first gate insulating film in this order (Fig. 36 –2(a));

b) forming a first protection insulating film consisting of one of a single layer film (Fig.39a (54, 42)) and a laminating film, the single layer film being a SiO film formed over the second conductive film (Col.12, lines: 30-35), and the laminating film being a SiN film formed over the SiO film Col.12, lines: 50-55);

c) patterning the first protection insulating film and thereby forming an etching mask consisting of the first protection insulating film;

d) patterning the second conductive film the second gate insulating film and the first conductive film in this order by dry etching using the etching mask as a mask (Col.11, lines: 50-55 and Col.12, lines: 35-40), and thereby forming a plurality of gate electrodes that each have a floating gate electrode (50) consisting of the first conductive filmCol.11, lines: 50-65) and a control gate electrode (55A) consisting of the second conductive film (52 and 53) and that each have a laminating structure in which an upper portion of the gate electrode is covered with the first protection insulating film (54, 42).

e) forming a etching prevention film consisting of a SiN film on both sidewall portion of the first protection insulating film patterned, after step (c) and before the step (d) or after step (d) (Col.12, liens: 50-55);

f) introducing impurities into the main surface of the semiconductor substrate located between sidewall portions facing each other in the plurality of gate electrodes, and thereby forming source and drain regions (Col.12, lines: 45-55);

g) treating a surface of the semiconductor substrate by using etchant containing HF acid after step (F) and thereby cleaning the first gate insulating film located between the sidewall portions which face each other in the plurality of gate insulating film (Col.6, lines: 5-10).

h) covering an upper portion of both sidewall portions of the gate electrode (50) and forming a second protection insulating film consisting of a SiN film having such a thickness as to partially embed a region between the sidewall portions which face each other in the plurality of gate electrodes (Fig.37 (a) (51));

i) forming on an upper portion of the second protection insulating film, an interlayer insulating film consisting of SiO and embedding with the interlayer insulating film, the region

between the sidewall portions which face each other in the plurality of gate electrodes (Fig.37 (a) (51)- 51 is an ONO film and therefore includes both an N and O layer);

j) etching the interlayer insulating film and second protection insulating film located between the sidewall portions which face each other in the plurality of gate electrodes (51), and thereby forming a first connection hole (Fig.39 (56))for exposing a surface of the source region and a second connection hole for exposing a surface of the drain region (56); and

k) forming a third conductive film electrically connected to the source region inside the first connection hole (Fig.43 (a) (58)), and forming a fourth conductive film electrically connected to the drain inside the second conductive hole (Fig.43(a) (64)).

In reference to claim 20, Hashimoto teaches wherein the third conductive film formed in the first connection hole functions as past of a source line (Col.13, lines: 5-15), and the fourth conductive film functions as a data line (Col.13, lines: 20-25).

In reference to claim 21, Hashimoto teaches wherein the plurality of electrodes constitutes a memory cell carried out by injecting a charge into the floating gate and erasing form the memory cell is carried out by discharging to the substrate the charge injected into the floating gate (Col.11, lines: 10-20).

In reference to claim 22, Hashimoto teaches wherein the flash memory is NOR type flash memory (Col.4, lines: 32-45).

In reference to claim 23, Hashimoto teaches wherein each of the at least one pair of laminating structure bodies constitutes a memory cell of the flash memory and writing is carried out by injecting (Col.11,lines: 10-20 and Col.13, lines: 20-25).

In reference to claim 24, Hashimoto teaches wherein the flash is an NOR type flash memory (Col.4, lines: 32-45).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (703) 308-6425. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1500.

LMS
November 26, 2002

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800